Proceedings of the International Conference on Green Computing and Engineering Technologies 2015

GYANCITY RESEARCH LAB

PRESENTS

INTERNATIONAL CONFERENCE ON GREEN COMPUTING AND ENGINEERING TECHNOLOGY

ON 25-26 July 2015

Radisson Royal Hotel Sheikh Zayed Road, Dubai, UAE.

Our Next Conference :

Editors
D. M. Akbar Hussain, G. S. Tomar, Bishwajeet Pandey

ISBN- 978-81-938900-0-4

Chair Message:

As a chair I have the honor to welcome you with great respect and enthusiasm to the International
Conference on Green Computing and Engineering Technology ICGCET-2015 to be held at Radisson Royal Hotel, Dubai on 25 – 26 July 2015. It is the first conference hosted by Gyancity Research Lab and as a founder member I hope that we will continue to provide such forums in future as well. ICGCET intended to attract innovative technical and scientific work in the field of Green Computing Engineering Technology. The response to the conference was over whelming and I am proud to state that we have really good quality contributions and I am sure as a participant you will share the same sentiment later.

As a chair and on behalf of the organizing committee I sincerely hope that ICGCET will offer a great venue at Dubai to the participants coming from different parts of the world to share and contribute in the area of green Computing Engineering Technologies. We hope to provide a good platform to the participants of ICGCET where not only they meet together and share their vision and ideas but also fertilize their thoughts in the ever-growingfield of Green Computing Engineering Technologies.

I am also confident that our keynote speakers will be able to enrich your knowledge during the conference and I wish you a very pleasant and enjoyable stay in Dubai.

Best wishes.

D. M. Akbar Hussain, Aalborg University Denmark.

Table of Contents

Chair Message: 2
Conference Information: 5
General Chair 5
Program Committee Chairs 5
International Programme Committee Member 6
Publication Chair 6
Advisory/Steering Committee 6
Technical Programme Committee Member 7
Co-Convener 8
Schedule: 9
Abstract of Paper Selected For 10
Presentation 10
SSTL IO Standard Based Energy Efficient Digital Clock Design on 28nm FPGA 10
HSTL IO Standard Based Energy Efficient FIR Filter Design on 28nm FPGA 11
Estimating Normalized Attention of Viewers on Account of Relative Visual Saliency of faces (NRVS) 12
Insertion - Deletion as informative characters in DNA barcoding 13
Cohort Selection of Specific User Using Max-Min-Centroid-Cluster (MMCC) Method to 14
Enhance the Performance of a Biometric System 14
Developing High Performance Web Execution Model Using OOPS and Procedural Programming 15
A Study of Today's A.I. through Chatbots and Rediscovery of Machine Intelligence 16
All Optical Regeneration for Optical Communication Network Using 3R Regeneration and Phase sensitive amplifier 17
Thermal aware Internet of Things Enable Energy Efficient Encoder Design for security on FPGA 18
Efficient Approach for Designing Gesture Controlled Robotic Arm 19
FPGA Based Energy Efficient Universal Asynchronous Receiver Transmitter Design Using 20
Thermal Scaling 20
Interconnected interface enhanced electrical properties of graphite in bio-based epoxy from insulating to conductor composites 21
Low Power Techniques for Digital System Design 22
Energy Efficient Design of Hyper Transport Protocol based Laser Driver using Low-Voltage Differential Signaling 23
Proposing a Algorithm for finding repetitive patterns in web dataflow 24
Capacitance Scaling Based Energy Efficient and Tera Hertz Design of Malayalam Unicode Reader on FPGA 25
COMPARATIVE STUDY FOR BIOGAS PRODUCTION FROM DIFFERENT WASTES 26
A Novel Hybrid Locomotion Mechanism for Small Mobile Robot 27

A novel optimal RFID network planning by MC-GPSO 28
IO Standards based Energy Efficient Room Temperature Sensor design 29
Phosphorus Removal from Urban Wastewater via Chemical and Combined Treatment against eutrophication of Receiving Environments 30
I/O Standards Based on Green Communication Using Fibonacci Generator Design on FPGA 31
Hardware Implementation of an Eco-Friendly Electronic Voting Machine 32
Future Perspective and Current Aspects of Internet of Things Enable Design 33
Analysis of Thermal Stability of Energy Efficient Arithmetic Circuit Design on Different FPGA 34
Energy Efficient Clean and Green IT: Concepts and 35
Approaches 35
Potential and Viability of Stand Alone Solar PV Systems for Rural Electrification 36
Comparative Analysis between Multi-grid MEMS Structure and Inter-digital Electrodes for 37
Moisture Measurement 37
Collaborative Optimal Reciprocal Collision Avoidance for Mobile Robots 38
Energy Efficient Memory Design Using Low Voltage Complementary Metal Oxide 39
Power Consumption Analysis of BCD Adder Using XPower Analyzer on VIRTEX FPGA 40
A Comparison of the 3DES and AES Encryption Standards 41
Thermally Aware LVCMOS Based Low Power Universal Asynchronous Receiver Transmitter Design on FPGA 42
Analysis of Classical Controller by Variation of Inner-Loop and Controller Gain for Two-Level Grid-Connected Converter 43
WIRELESS POSITION TRACKING OF A DTMF BASED MOBILE ROBOT USING GSM AND GPS .. 44
THE EMERGING ELECTRONIC MEDIA AND ITS INFLUENCE ON THE READING HABIT OF SCHOOL CHILDREN IN NIGERIA 45
SSTL Based Power Efficient Implementation of DES Security Algorithm on 28nm FPGA 46
Wi-Fi to Li-Fi Migration accelerating for next generation systems: Approaches and applications 47
Iterative Linear Quadratic Regulator (ILQR) Controller for Trolley Position Control of Quanser 3DOF Crane 48
Examination of Thai Construction Safety Factors using the Analytic Hierarchy Process 49
Data Protection in Clouds using Two Stage Encryption 50
Optimization of Solar Photo Voltaic Power Generation Efficiency by Cooling System 51
Developing an Efficient Desktop Application of Hospital Care Management System using Java and Database Management 52
28nm FPGA Based Power Optimized UART Design Using HSTL I/O Standards 53
Two Level Voltage Source Grid Connected Inverter for Solar Photovoltaic 54
Our Next Conference 55

Conference Information:

We are grateful for your contribution in International conference on Green Computing and Engineering Technology (ICGCET) 2015. The venue of Conference is Radisson Royal Hotel, Dubai. It is situated on Sheikh Zayed Road, Dubai, and UAE.

The conference is going tobeheld on 25-26 July 2015 in Dubai. The main objective of ICGCET'15 is to present the research from different areas of science and technology. This conference provides a platform for researchers and scientists across the world to exchange and share their experiences and research results about all aspects of electronics and information technology. This conference also provides an opportunity to interact and establish professional relations for future collaboration. The conference aims to promote innovations and work of researchers, engineers, students and scientists from across the world on Advancement in electronic and computer systems. The basic idea of the conference is what more can be done using the existing technology. In Today's world electronic and computer systems plays an important role for future's innovation. These systems involve a very wide area for research.

We are pleased to inform that we received more than 200 papers. In order to maintain publication ethics and practices of Scopus Index Journal, we accepted only 60 papers (30% acceptance rate). All accepted papers have been submitted to following SCOPUS Index Journal. Paper will be available online by end of 2015.

Following are the SCOPUS indexed journals in which papers has been submitted:

- **International Journal of Software Engineering and Its Applications**
- **International Journal of Control and Automation**
- **Indian Journal of Science and Technology**
- **International Journal of Multimedia and Ubiquitous Engineering**
- **International Journal of Security and Its Applications**
- **International Journal of Smart Home**

We are grateful for our chair for their constant guidance and motivation of more than 300 committee members for quality in review and also deliver high performance as per global standards. Few papers are sent to other Scopus indexed journals also.

General Chair

Prof G S Tomar, MIR Lab, Gwalior, India
Prof D. M. A. Hussain, Aalborg University, Denmark

Program Committee Chairs

Manisha Pattanaik, Indian Institute of Information Technology and Management, Gwalior, India

Bikram K.Bahinipati, Amity School of Engineering and Technology, Amity University Madhya Pradesh. Bishwajeet Pandey, Chitkara University, India

International Programme Committee Member

- Jens Bo Holm-Nielsen, Aalborg University, Denmark
- Haoping Wang, Nanjing University of Science and Technology, Nanjing, China
- Akshay Kumar Rathore, National University of Singapore, Singapore
- Abdelhalim Zekry, Ain Shams University, Cairo, Egypt
- BS Chowdhry, Mehran University of Engineering and Technology, Sind, Pakistan
- Muhammad Faiz Liew Abdullah, Tun Hussein Onn University of Malaysia
- Teerath Das, Gran Sasoo Science Institute, Italy
- Md.Mahbub-E-Noor, University of Barisal, Bangladesh.
- Tanesh Kumar, University of Oulu, Oulu, Finland
- Nitish Rajoria, Keio University, Japan
- Noor Zaman, King Faisal University, Saudi Arabia

Publication Chair

- Jens Bo Holm-Nielsen, Aalborg University, Denmark
- Pradip Swarnkar, Indian Institute of Information Technology and Management, Gwalior, India
- Pardeep Kumar, Associate Professor, CSE, QUEST Nawabshah, Pakistan
- Khyati Nanda, Chitkara University Research and Innovation Network, India
- Yusri Yusof, Tun Hussein Onn University of Malaysia

Advisory/Steering Committee

- Anupam Shukla, Indian Institute of Information Technology and Management, Gwalior, India Swarn Singh, Sri Venkateswara College, Delhi University, India.
- Jitender Grover, M.M. University, Sadopur, Ambala (Haryana), India
- Ajay Kumar Chauhan, Institute of Management Technology, Ghaziabad
- Shivani Malhotra, Chitkara University, Chandigarh, India
- Mahua Bhatacharya, Indian Institute of Information Technology and Management, Gwalior, India
- Sheifali Gupta, Chitkara University, Chandigarh, India
- Atiqur Rahman, South Asian University, Bangladesh
- Muhammad Aamir, Mehran University of Engineering & Technology, Pakistan.
- Dr Syed Hyder Abbas Musavi, Indus University, Karachi, Pakistan
- Anu Singla, Chitkara University, Chandigarh, India
- Gaurav Verma, Jaypee Institute of Technology, India
- Jagdish Kumar, Scientist, National Knowledge Network Labs, India

- Md Hashim Minver, Addalaichenai National College Of Education, Srilanka
- Vijay Shri Chaurasia, National Institute of Technology, Bhopal, India
- Viswam Parthiban, National University, Singapore
- Harsh Sohal, Chitkara University, Chandigarh, India
- V B Taneja, Academic Director, C-DAC, Noida, India
- Deepti Arora, DESIDOC, DRDO, India
- Vishal Jain, Bharti Vidyapeeth, New Delhi, India
- Binod Kumar, MCA-Director, Jayawant Technical Campus (JSPM's Group), University of Pune
- Irfan Ahmed Halepoto, Mehran University of Engineering and Technology, Sind, Pakistan
- SM Tanvir Siddiquee, Tsinghua University, China
- Bhagwan Das, Tun Hussein Onn University of Malaysia
- Gurpreet Singh, Yamuna Institute of Engineering & Technology, Yamuna Nagar, India.
- Roopa Kulkarni, GIT, Belgaum, India
- Abhineet Anand, UPES, Dehradun, India

Technical Programme Committee Member

- Aditi Moudgil, Chitkara University, Chandigarh, India
- Akash Kumar, National University of Science and Technology, Islamabad, Pakistan
- Amanpreet Kaur, Chitkara University, Chandigarh, India
- Amanpreet Sandhu, Chitkara University, Chandigarh, India
- Aniket Ingavale, Trinity College of Engineering and Research, Pune
- Ashutosh Singh, Motilal Nehru National Institute of Technology, Allahabad, India
- Ashvinikumar Dongre, G.H. Raisoni College of Engineering, Nagpur, India
- Bhanu Sharma, Chitkara University, Chandigarh, India
- Chhavi Saxena, Maharana Pratap College Of Technology, Gwalior, India
- Deepa Singh, ABV-IIITM Gwalior
- Deepak Baghel, Researcher, MPCT, Gwalior
- Deepshikha Bhatt, Chitkara University, Chandigarh, India
- Dharmendra Prasad, IIT Varanasi, India
- Furqan Fazili, Islamic University of Science & Technology, Awantipora, India
- Harsh Vishwakarma, Tata Consultancy Services, India
- Jyotsana Yadav, Gwalior Engineering College, India
- Kanika Garg, Chitkara University, Chandigarh, India
- Kavita Goswami, Chitkara University, Chandigarh, India
- Kulbhushan Sharma, Chitkara University, Himachal Pradesh, India
- Kumar Gaurav, Researcher, South Asian University, India
- Kumar Satyam, Fast Conversion Lab, New Delhi
- Love Kumar, Bridge Network

- Manoj Bhatt, HCL Noida
- Manish Kumar Singh, IIT Patna, India
- Md.Mahbub-E-Noor, University of Barisal, Bangladesh.
- Meenakshi Bansal, Chitkara University, Chandigarh, India
- Payal Arora, Chitkara University, Himachal Pradesh, India
- Prabhat Ranjan Singh, Researcher, South Asian University, India
- Pradeep Kumar Bhale, Govt. College OF ENGINEERING, Aurangabad, India
- Rajendra Aaseri, Lovely Professional University, Jalandhar, India
- Ravikant Kumar, Central University, Hyderabad
- Ravinder Kaur, Punjab University, India
- S J Bendra, South Asian University, Srilanka
- S.M.M. Islam, South Asian University, Bangladesh
- Sachin Sharma, Sharda University, Gr. Noida, India
- Shaina Verma, Chandigarh Group of Colleges, Mohali, India
- Shanti Bhushan, IIIT Gwalior, India
- Shivani Madhok, Chitkara University, Chandigarh, India
- Subham Gargarish, Chitkara University, Chandigarh, India
- Sujit Thakur, Researcher, South Asian University, Nepal
- Sunny Singh, Chitkara University, Chandigarh, India
- Sweety Dabbas, Maharaja Surajmal Institute, Janakpuri, Delhi
- Tarandeep Kaur, Infosys, India
- Urmala Rai, Aga Khan Hospital, Karachi, Pakistan
- Veer Pratap Singh, National Institute of Technology, Bhopal
- Yogesh Singh, Indian Institute of Information Technology and Management, Gwalior, India

Convener

Kartik Kalia, Chitkara University Research and Innovation Network, India

Co-Convener

Sumita Nagah, Gyancity Research Lab, Gwalior, India

Schedule:

Day 1: 25-July-2015

8:30 Am	Reporting at Registration Desk
09:00 Am	Inaugural Speech by Both Chair Prof D M Akbar Hussain and Prof Geetam S Tomar
09:30-10:15 Am	First Keynote by Prof G. Sanyal and Paper Presentation
10:15-11:00 Am	Second Keynote by Prof M F L Abdullah and Paper Presentation
11:00-11:15 Am	Coffee Break
11:15-1:30 Pm	Paper Presentation
1:30-2:30 Pm	Lunch
2:35-3:15 Pm	Third Keynote By Prof. Mohsin Jamil and Paper Presentation
3:15-4:30 Pm	Paper Presentation
4:30-4:45 Pm	Coffee Break
4:45-5:30 Pm	Paper Presentation
5:30-6:30 Pm	Fourth Keynote by Professor Jitendra Agarwal

Day 2: 26-July-2015

8:30 Am	Reporting at Registration Desk
9:00-10:00	Keynote by Prof Sanjeev Sharma
09:30-1:30 Am	Paper Presentation
1:30-2:30 Pm	Lunch
2:30-4:30 Pm	Paper Presentation
4:30-5:30 Pm	Ending Ceremony

Abstract of Paper Selected For Presentation

Paper Id	Title, Authors, Affiliations and Abstracts
4	SSTL IO Standard Based Energy Efficient Digital Clock Design on 28nm FPGA Shivani Madhok[1], Navdeep Singh[1], Furqan Fazili[2], Sumita Nagah[3], Sweety Dabas[3], Ravider Kaur[4] Chitkara University, Chandigarh, Punjab, Islamic University of Science &Technology, Awantipora, India Gyancity Research Lab, New Delhi, India, Punjab University, Chandigarh, India shivanimadhok0@gmail.com, rkrozy5@gmail.com furqanfazili@gmail.com, sumi@gyancity.com, *Abstract*- In this paper we have aimed to have an energy efficient digital clock design. Digital clock is a type of clock that displays time digitally. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family using different SSTL IOStandards. Comparison between different SSTL IOStandard has been done to achieve minimum IO power. Via SSTL technology, we achieve green computing with respect to low voltage impedance. In this work we are testing our digital clock design with different SSTL IOStandards such as SSTL15, SSTL18_II, SSTL135, SSTL12, and SSTL18_I. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. The design consists of five inputs and six outputs. At the end, we concluded that there is 24-35% saving in total power dissipation with 1.2 GHz when compared with 2.2 GHz.

5

HSTL IO Standard Based Energy Efficient FIR Filter Design on 28nm FPGA

Shivani Madhok[1], Navdeep Singh[1], Jasleen Kaur[1], Khyati Nanda[1], Sweety Dabas[2], Minal Dhankar [2]
[1]Chitkara University Research and Innovation Network
[2]Maharaja Surajmal Institute of Technology, Janakpuri, Delhi, India
shivanimadhok0@gmail.com, navisidhu111@hotmail.com, raghbirsingh1962@gmail.com, khyati729@gmail.com, sweety.dabas@gmail.com, minal.dhankar@gmail.com

Abstract- In this research paper, we have designed an energy efficient FIR Filter that is very much useful in digital signal processing (DSP). FIR isa finite impulse response (FIR) filter is a filter whose impulse response is of finite duration. In this paper we have aimed to design a FIR Filter that consists of three inputs and one output. The three inputs are input data that is 8 bit or 1 byte (finite), clock and reset. The output is 18 bits (finite) wide. The code has been implemented in Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform. The design has been tested on Kintex-7. Power analysis has been done at different operating frequencies. . In this paper we have done frequency scaling technique to obtain energy efficient design. The temperature has been kept constant that is 25 degree Celsius.Airflow and heat sink are main parameters while analyzing the thermal dissipation in the circuit [12]. In this work we have taken constant value of air flow and heat sink. Airflow has been kept 250 LFM and medium Heat sink. In this paper we have taken HSTL (High Speed Transceiver Logic) IOSTANDARD. HSTL family consists of HSTL _I, HSTL_II, HSTL_I_18 and HSTL_II_18, HSTL_I_12 and the analysis has been done on these IO standards. We can conclude that there can be 23-33% saving of total power dissipation by using frequency scaling technique.

11

Estimating Normalized Attention of Viewers on Account of Relative Visual Saliency of faces (NRVS)

Ravi kant kumar[1*], Jogendra Garain[2], Goutam Sanyal[3], Dakshina Ranjan Kisku[4]
National Institute of Technology Durgapur, Durgapur – 713209, West Bengal, India
{vit.ravikant, jogs.cse, nitgsanyal, drkisku}@gmail.com

Abstract- Humans psychological and behavioral understanding often lead to make natural decision which accurately identifies and remembers the faces which are highly appreciated or criticized by themselves in comparing to the normal viewed faces, in terms of beauty, ugliness or unique appearance. It happens due to human psychology of being biased towards the salient face in the process of face recognition and identification. This paper attempts a novel method to measure, how our attention is more restricted towards some particular faces in the crowd. This restricted attention is strongly guided by the relative visual saliency of these faces. In this paper, normalized relative visual saliency (NVRS) of the faces is evaluated using their intensity values modulated with respective spatial distance. Experiment has been carried out on test image dataset via bottom up approach. The experimental results are found to be encouraging and accuracy has also been measured exhibiting efficacy of the proposed approach.

12

Insertion - Deletion as informative characters in DNA barcoding

Goutam Sanyal [1], Asim Kumar Mahadani[2], Pradosh Mahadani[3], Partha Bhattacharjee[4]

[1]National Institute of Technology, Durgapur, West Bengal,India
[2]Bankura Unnayani Institute of Engineering, West Bengal, India
[3]ICAR- National Research Center for Orchids, Pakyong, Sikkim, India
[4]Central Mechanical Engineering Research Institute,Durgapur,India nitgsanyal@gmail.com, asimmahadani@yahoo.com, pmahadani@gmail.com, partha_cmeri@yahoo.com

Abstract- DNA barcoding involve rapidly sequencing the standardized region from the genome for species identification and this homologous sequence information plays an important role to resolve the phylogenetic issues. However in case of complex groups, incorporation of insertion and deletion (Indel) informative sites in DNA barcode sequences are becoming more important due to low substitution rate. Indels are largely ignored in phylogenetics analysis and removed from sequence alignment assigning them a missing data. We review the current trends on mining the indels analysis, focusing especially on the topics of rapidly evolving indel containing loci and methods of indel treatment for phylogenetic relationship. Among the indel coding methods, Simple indel coding is easy to implement in indels contain sequences. But, this method does not utilized the all the available information and Complex Indel Coding rules are very difficult to translate into a clearly formulate algorithm for determining the values. But this coding method suffers from internal inconsistence when a long indel has a number of shorter subset indel and triangular in equality exists. However, SIDIER software package infer evolutionary relationships based on both the indels and substitutions. SIDIER is promising software for intra and inter specific calculation in DNA barcode studies as well as to infer phylogenetic relationships.

13

Cohort Selection of Specific User Using Max-Min-Centroid-Cluster (MMCC) Method to Enhance the Performance of a Biometric System

Jogendra Garain[1], Ravi Kant Kumar[2], Goutam Sanyal[3], Dakshina Ranjan Kisku[4]
National Institute of Technology Durgapur, Durgapur – 713209, West Bengal, India
{jogs.cse, vit.ravikant, nitgsanyal, drkisku}@gmail.com

Abstract- Selection of cohort models plays a vital role to increase the accuracy of a biometric authentication system as well as to reduce the computational cost. This paper proposes a novel approach for cohort selection called Max-Min-Centroid-Cluster (MMCC) method. The clusters of cohorts are generated by K-means clustering technique. The union of the clusters having largest and smallest centroid value is taken as cohort subset. The cohort scores, after normalization using different cohort based score normalization techniques, are used in authentication process of the system. Evaluation has been carried out on FEI face datasets. The performance of this novel methodology is analyzed using T-norm and Aggarwal (max rule) normalization techniques.
Experimental results exhibit the efficacy of the proposed method.

16

Developing High Performance Web Execution Model Using OOPS and Procedural Programming

Mansee Jain[1], manisha.oswal56@gmail.com[1], Devashish Puri[1],
mannatnanda1@gmail.com[1],
rainavreet@gmail.com[1], Ahmad Shah Abdali[2]
Department of Computer Science, Chitkara University, Punjab, India[1]
South Asian University, Delhi[2]
mansee.jain@chitkara.edu.in[1], manisha.oswal56@gmail.com[1],
devashishpuri@gmail.com[1], mannatnanda1@gmail.com[1],
rainavreet@gmail.com[1],ahmadshah.2008@hotmail.com[2]

Abstract- Now, human progress is on the verge of virtual world with the introduction of YouTube,
Wikipedia and Facebook. In this work, we are using the best feature of both OOPs and Procedural Programming in order to achieve the goal of developing high performance web execution model. Client and server are integral part of any web-based model. Here, we are integrating compiler and program in web based model and finally come with high performance web execution model. High performance system means taking less time in compare to other existing traditional models. Many web based service like YouTube and Wikipedia are benefitted by taking advantage of our laziness. We want everything on the go, just in our hand-held computer. This work is also solving the beginners' laziness problems like setup of Programming Environment such as compilers etc. If our education system is being shifted online, then this may turn out a big setback in learning process. Thus, we are providing compiler on the go so that the learning process is not interrupted by unavailability of resources (Our whole system is client-side) and of course by the laziness of people.

17

A Study of Today's A.I. through Chatbots and Rediscovery of Machine Intelligence

Anirudh Khanna[1], Bishwajeet Pandey[1], Kushagra Vashishta[1], Kartik Kalia[1], Bhale Pradep Kumar[2], Teerath Das[3]

[1] Chitkara University, Punjab, India
[2] IIITM, Gwalior, India
[3] Gran Sasoo Science Institute, Italy

anirudhkhanna.cse@gmail.com, bishwajeet.pandey@chitkara.edu.in, kushagravashishta@gmail.com, kartikalia4@gmail.com, bhalepradeepkumar.iiit@gmail.com , teerath.sitani@gmail.com

Abstract- Artificial Intelligence in machines is a very challenging discussion. It involves the creation of machines which can simulate intelligence. This paper discusses some of the current trends and practices in AI and subsequently offers alternative theory for improvement in some of today's prominent and widely accepted postulates. For this, focus on the structuring and functioning of a simple A.I. system - chatbots (or chatter bots) is made. The paper shows how current approach towards A.I. is not adequate and offers a new theory that discusses machine intelligence, throwing light to the future of intelligent systems.

18

All Optical Regeneration for Optical Communication Network Using 3R Regeneration and Phase sensitive amplifier

BhagwanDas[1], M.F.LAbdullah[1], Mohd ShahNorShahida[1], QadirBukhsh[1]
UniversitiTun Hussein Onn Malaysia (UTHM)
he130092@siswa.uthm.edu.my

Abstract- Nonlinear optical effects in fibers occur via ultrafast Kerr nonlinearity, offers a flexible framework within which numerous signal-processing functions can be accomplished. When high power launched in optical fiber, several nonlinear transmission impairment such as amplitude noise, phase noise, power spectral losses, that degrade the performance of optical communication system. All optical regeneration is one of the solutions to mitigate transmission impairments instead of optical to electrical conversion. In this paper, all optical regeneration is demonstrated for 10Gb/s DPSK system using 3R regeneration and Phase sensitive amplification to mitigate amplitude and nonlinear phase noise form10G noisy DPSK transmission system. Bit error rate of $10^{-11}$is achieved at power penalty of 6 dB. The system is developed and tested using optisystem. The developed all optical regeneration system is very demanding for long distance transmission in high-speed communication systems.

25

Thermal aware Internet of Things Enable Energy Efficient Encoder Design for security on FPGA

Deepa Singh[1], Kanika Garg[2], Ravneet Singh[2], Bishwajeet Pandey[2], Kartik Kalia[2], Hasmatullah Noori[3]
[1]Department of IT, ABV-IIITM, Gwalior, India
[2]Department of Computer Science, Chitkara University, Chandigarh, India
[3]Department of CSE, South Asian University, Delhi, India
deepasingh.iiitm@gmail.com, kanika.garg@chitkara.edu.in, gyancity@gyancity.com, kartikkalia4@gmail.com, satshriakal555@gmail.com, hashmatullah.noori2010@gmail.com

Abstract- In this work, we are going to use thermal aware approach in Encoder design and also testing thermal stability by working on different ambient temperatures 298.15K, 308.15K, 318.15K, 328.15K, 338.15K and 348.15K and 358.15K. We have observe the compatibility of our device with wireless network by working on different I/O standards (LVCMOS15 and LVCMOS25) . There is 30.29% reduction in leakage power, when we scale down temperature from 358.15K to 298.15K using LVCMOS15 as I/O standard on 40nm Virtex FPGA. Leakage power is calculated for 65nm FPGA and 90nm FPGA as well .In this work, we are using Verilog Hardware Description Language.

26

Efficient Approach for Designing Gesture Controlled Robotic Arm

Shivani, Shagun Gaur,Paresh Khaneja,Rashmi Sharma,Simranpreet Kaur,Mehakpreet Kaur
Department of ECE, Chitkara University, Chandigarh, India
shalu16sharma@gmail.com, shagungaur74@yahoo.co.in, Pareshkhaneja@gmail.com, rashmisharma1505@gmail.com, simranchhabra2394@gmail.com, mehakpreet_26july@yahoo.com

Abstract- Gesture Controlled Robot is a robot that can be moved according to our limb movements. All we need to do is just wear a gesture device which consists of a sensor such as accelerometer. The sensor mounted on your hand will judge the movement of hand in a particular direction which will result in the movement of the robot in the direction of the hand movement. In this era of modern technology, technology has decreased working hours and has made complicated operations more effortless. Robotics is a very vast field that has helped us make some wonderful machines that assist us in our daily lives or even commercially. Typical industrial robots usually perform tasks that are difficult, dangerous, too complex or dull. They lift heavy weights, and a lot of manual work such as welding can be done using robots. They can perform the same course of action in lesser time with more accuracy. This robotic arm is focused on developing a device by interfacing the hardware with software and creating something which makes the performance of complicated activities comfortable. Though the working of a robotic arm is very simplified, the implementation of this arm requires a good knowledge of Engineering Mechanics, Arduino platform, Electronics Devices mainly sensors and Embedded Systems as well.

27

FPGA Based Energy Efficient Universal Asynchronous Receiver Transmitter Design Using Thermal Scaling

Rashmi Sharma[1], Shivani Sharma[1], Paresh Khaneja[1], Navya Bhasin[1], Vanshaj Taxali[1], Vaashu Sharma[2]
[1]Department of electronics and communication, Chitkara University, Chandigarh, India
[2]Department of electronics and communication, NIT Hamirpur, Hamirpur, India
{rashmisharma1505, shalu16sharma, pareshkhaneja, navya27bhasin, vanshaj1994}@gmail.com,
vaashu.sharma@gmail.com

Abstract- This paper throws light on the behavior of the UART in response to the variations in the junction temperature. Analysis has been done to find the most ideal temperature range for the operation of the UART. After all the calculations, deduction comes to a point that lowering the temperature values increases the efficiency of the UART significantly since the losses due to the leakage power are reduced to a minimum value when the temperature is decreased. Significant reduction in the percentage of leakage power is seen as the temperature is lowered. Implementation has been done on the FPGA generations Virtex-6, Virtex-5, Virtex-4 using XILINX simulator and Verilog Hardware Description Language. Different reduction percentages have been observed within a range of 8% to 37.4% for the leakage power and 16.8% to 69.3%for the ambient temperature as the results are obtained for frequency values of 1GHz and 1MHz. Thus various power loss parameters have been studied to get the best energy efficient UART.

28

Interconnected interface enhanced electrical properties of graphite in bio-based epoxy from insulating to conductor composites

Anika Zafiah M. Rus[1], Nur Munirah Abdullah[1], M.F.L Abdullah[2]
Sustainable Polymer Engineering, Advanced Manufacturing and Material Center (AMMC), Faculty of
Mechanical and Manufacturing Engineering,
2 Department of Communication Engineering, Faculty of Electrical and Electronic Engineering,
Universiti Tun Hussein Onn Malaysia, 86400 Parit Raja, Batu Pahat, Johor, MALAYSIA zafiah@uthm.edu.my,
nurmunirahabdullah87@gmail.com,faiz@uthm.edu.my

Abstract- The fabrication and characterization of composite films of graphite/bioepoxy is disclosed. Thin films of ~0.1 mm thick are prepared using a simple solution mixing with mass proportion of 1/0.5 (biomonomer/ Methylene Diphenyl Diisocyanate, MDI), upon differ treated graphite weight loading (5 wt.%, 10 wt.%, 15 wt.%, 20 wt.%, 25 wt.%, 30 wt.%) and drop casting at room temperature. The morphologic study by FE-SEM shows a homogeneously dispersed and strong interface between the graphite and the bioepoxy material. Ultraviolet-visible (UV-vis) spectrophotometer are performed to evaluate the changes in adsorption spectra arising with the increasing of graphite weight loading (wt.%) into the bio-based matrix. An eye opening I-V characteristic of the thin films where the percolation threshold occurs at higher graphite loading (20 wt.%, 25 wt.% and 30 wt.%) gives conductivity of 10^3- 10^4 S/m. Whilst lower graphite loading (5 wt.%, 10 wt.% and 15 wt.%) somehow need further discussion. The influence of graphite in bioepoxy materials is paramount as it across insulatingsemiconductor-conductor applications.

30

Low Power Techniques for Digital System Design

Gaurav Verma, Dr. Manish Kumar, Dr. Vijay Khare
Department of ECE, Jaypee Institute of Information Technology, Noida (U.P.)-India gaurav.verma@jiit.ac.in, manish.kumar@jiit.ac.in, vijay.kumar.jiit.ac.in

Abstract :The proliferation of reconfigurable hardware like (FPGAs) put a challenge in front of designers to implement fast and low powered digital designs. Main drawbacks of FPGAs are the complex circuitry which makes them less efficient as compared to ASIC (application specific integrated circuits). Although appropriate to scaling in CMOS technology reduce the power required for performing the known job, it increase clout indulgence for each part of region. At similar instant request of low power application is swelling due to increase of smart devices and increasing energy costs. Since power consumption is an extremely significant issue in digital classification of designs, so the authors have presented & analyzed some power reduction techniques that can be targeted at different levels of design hierarchy for different target platform. The authors would also discuss concept of ACPI module designed for newer operating systems, which provides basic power management facilities to save system power.

31

Energy Efficient Design of Hyper Transport Protocol based Laser Driver using Low-Voltage Differential Signaling

BhagwanDas[1], M.F.LAbdullah[1], Mohd ShahNorShahida[1], QadirBakhsh[1]
UniversitiTun Hussein Onn Malaysia (UTHM)
he130092@siswa.uthm.edu.my

Abstract- In this paper, laser driver circuit is designed using current mode logic for safe mode interface of laser with devices attached ahead. Furthermore, energy efficient design is realized on FPGA virtex-6 using Low Voltage Differential Signaling technique. The energy efficient design is tested on Hyper Transport Protocol IO standard on FPGA that includes HTP 1.1, HTP 2.0, HTP 2.5, HTP 3.0 and HTP 3.1 having operating frequencies 1 GHz, 10 GHz, 100 GHz, 1 THz and 10 THz respectively. In LVDS, the four voltage swing values are taken2.5V, 1.2V, 0.9V and 0.3V. Laser driver is operated at mentioned hyper transport protocols for each voltage swing value. It is extracted that when laser driver is operated at all HTPs on voltage swing 0.3V; the maximum power reduction is recorded. For HTP 1.1.87%, for HTP 2.0.85%, for HTP 2.5.85%, for HTP 3.0.86% and for HTP 3.1. 86% power reduction is recorded at LVDS voltage swing 0.3V in comparison with LVDS voltage swing 2.5V. The main contribution of this work is that energy efficient design of laser driver is proposed that consume less power when signal is transferred at different protocols having high frequenciesusing LVDS technique.This laser driver will be integrated with other optical components in system to provide green optical communication. The design is demonstrated using Xilinx 14.3 software package.

41

Proposing a Algorithm for finding repetitive patterns in web dataflow

Mohammad Rostami[1], Somayyeh Ehteshami[2] ,Fatemeh Yaghoobi[3], Farid Saghari[4], Samaneh Dezhdar[5]
[1]Member of Young Researchers Club, Islamic Azad University, Isfahan, Iran,
[2]Software Engineering Department, Shiraz, Iran
[3]Software Engineering Department, Isfahan, Iran
[4]Software Engineering
[5]Department, Tabriz, Iran
Software Engineering Department, Arak, Iran
mohammadrostami@dehaghan.ac.ir, es_010111@yahoo.com, fatemehyaghobi20@gmail.com, saghari@modiranyar.com, s.dezhdar@gmail.com

Abstract- Today, searching repetitive patterns on data flows is very important. By data flow we mean a type of data which is constantly produced in a very fast and unlimited manner. As a kind of these data we can name the report of clicks in computer networks. A repetitive pattern is a pattern which is available in a significant number of transactions. Finding repetitive patterns in data flows is a new and arguable issue in data mining as data is received in form of fast and continuous flow. Unlike static databases, flow mining faces a lot of problems including single review, requiring unlimited memory and high rate of input data.

A common way of searching repetitive patterns is the excess check of data which requires to be saved in memory. In addition, according to the features of data flows i.e. unlimited and fast production, it is not possible to save them in memory and hence techniques are needed which are able to process them online and find repetitive patterns. One of the most popular relative techniques is using sliding windows. It sadvantage is reduction of the consumed memory and increasein search speed.

In this paper, a new vertical display and an algorithm based on pins, called DBP-BA, are proposed to find repetitive patters in data flows. Since this new display without any additional task has a compact form, the proposed algorithm has a better performance than similar ones in terms of consumed memory and processing time. On the other hand, experiments support this matter.

44

Capacitance Scaling Based Energy Efficient and Tera Hertz Design of Malayalam Unicode Reader on FPGA

Amanpreet Kaur[1], Furqan Fazili[2] ,, Sunny Singh[1], Vaishali Sharma[1], Amandeep Singh[1], Md Hashim Minver[3]

Chitkara University, India[1]
Islamic University of Science and Technology, India[2] Addalaichenai National College of Education, Srilanka[3]

amanpreet.kaur@chitlara.edu.in, furqanfazili@gmail.com, sunny.sigh@chitkara.edu.in, vaishalisharma5.vs@gmail.com, amanhearthacker9@gmail.com, mhminver@gmail.com

Abstract- Malayalam is Kerala's official language, south-western region of India mainly speak this language, and very less research has been done for designing Malayalam Unicode reader. The Unicode range of characters for Malayalam script is 0D00–0D7F. In this work, we are focusing on the script of Malayalam language and its Unicode required for coding in Hardware Descriptive Language. This paper covers the hardware design and implementation of Malayalam Unicode Reader (MUR) for Kairali scripts on FPGA. This MUR design was tested with the device operating at frequency of 1THz, Capacitance has been varied from 1pF to 25pF with SSTL family (Stub Series Terminated Logic) with an interval of 5pf.

45

COMPARATIVE STUDY FOR BIOGAS PRODUCTION FROM DIFFERENT WASTES

Nabila Laskri[a], Nawel Nedjah[a]
Preparatory School of Sciences and Technology —23000 Annaba, Algeria; laskri_n@yahoo.fr (N.Laskri),nedjah_nawel@yahoo.fr (N.Nedjah)

Abstract- The bulk of our work was performing the anaerobic digestion of wastes rich in organic matter in a laboratory prototype. The two different substrates: the biodegradable waste from landfill and sludge from the wastewater treatment plant by natural lagoon. We surveyed the evolution of the degradation of organic matter of both experiments which are carried in a digester with a capacity one liter, sealed. During the experiments we followed themeasure of the COD (chemical oxygen demand), the volume of biogas formed during the digestion, the temperature and the pH. The biogas produced from the anaerobic digestion of the two substrates is flammable with a percentage of CH_4 more than 64%. Comparing the volume of biogas produced during the digestion of the two substrates of digestion we found that the volume collect from the sludge waste is greater than 10 times relative to the volume of biogas produced with organic matter in the landfill. The volume of biogas produced is always a function of the residence time of digestion and the concentration of organic matter in the experiment. The percentage of decrease in COD of the sludge was estimated at 87.3% and the substrate of the landfill is
82.44%.

48

A Novel Hybrid Locomotion Mechanism for Small Mobile Robot

Khalid Hasnan[1], Qadir Bakhsh[1], Aftab Ahmed[1], Bhagwan Das[1], Sanam Ayub[2]
Universiti Tun Hussein Onn Malaysia,Parit Raja, Batu Pahat, Johor, Malaysia
Riphah International University, Islamabad, Pakistan

khalid@uthm.edu.my , qadirquest@gmail.com, aftabgmik@gmail.com, he130092@siswa.uthm.edu.my, sanumayub@gmail.com

Abstract- A novel design of hybrid locomotion system for mobile robots is presented in this paper. The wheel and track type combined motion system used, which results as a hybrid locomotion mechanism that includes a robot flexible and versatile interchangeable locomotion. This robot has a switchover module (Track Tensioner unit) thathelps the robot to change wheel mechanism from track mechanism. The switchover module operated by means of rack and pinion mechanism, with the force exerted by pinion on mating rack. The switchover module slides upward and downward depends on the direction of pinion rotation. This hybrid mobile robot will be able to work in all type of terrains.

51

A novel optimal RFID network planning by MC-GPSO

Khalid Hasnan[1], Aftab Ahmed[1], Badrul-aisham[1], Qadir Bakhsh[1], Kashif Hussain[1], Kamran Latif [1]
Universiti Tun Hussein Onn Malaysia, 86400, Parit Raja, Batu Pahat, Johor, Malaysia khalid@uthm.edu.my, aftabgmik@gmail.com, aisham@uthm.edu.my, qadirquest@gmail.com, usitsoftrevised@gmail.com, engrkamranqureshi@gmail.com

Abstract- The fast development of RFID technology having challenging issues of the optimal deployment of RFID network are tags coverage, interference, economic efficiency and load balance. In this paper the novel approach of multi-colony global particle swarm optimization (MC-GPSO) algorithm was used to deploy minimum number of reader which covers all tags with minimum interference effect in large scale basis. The main aim of this algorithm is to divide the swarm in to multi-colony for achieving the optimal results as compared to the basic PSO. Simulation results show the optimal solution of RFID network planning (RNP).

53

IO Standards based Energy Efficient Room Temperature Sensor design

Shaina Verma[1], Rashmeet Kaur[1], Sanjima Rana[1], Divya Gaba[1], Heena[1], Sweety Dabas[2]
Department of ECE, Chandigarh University, Mohali (India)
shaina.verma16@gmail.com
Maharaja Surajmal Institute,
Delhi(India)
sweety.dabas@gmail.com

Abstract- In this work energy efficient room temperature sensor is designed using various IO standards. This design is implemented on Kintex-7 FPGA, XC7K70T device and FBG676 package. The simulator used is Xilinx 14.6 and Verilog is used as the verification language. The power analysis is done using XPower estimator. The various IO standards implemented in the design are HSUL_12, Mobile_DDR, PCI33_3 and SSTL18_II. The temperature scaling is being done for analyzing the behavior of circuit at different temperature values. The temperature is scaled from 50oC to 45oC, 40oC, 35oC, 30oC and 25oC. There is reduction of 17.39%, 65.22% and 91.30% in IO power when we migrate our design from SSTL18_II to HSUL_12, Mobile_DDR and PCI33¬_3 IO standards respectively. The maximum reduction in total power is achieved when the design is migrated from SSTL18_II to PCI33_3 IO standard. The reduction in total power is 26.32%, 24.69%, 22.72%, 20.83%, 18.87% and 16.95% at 25oC, 30oC, 35oC, 40oC, 45oC and 50oC respectively when the IO standard is migrated from SSTL18_II to PCI33_3.

55

Phosphorus Removal from Urban Wastewater via Chemical and Combined Treatment against eutrophication of Receiving Environments

Nawel Nedjaha, Nabila Laskria
Preparatory School of Science and Technology (EPST) —23000 Annaba, Algeria; emails: nedjah23nawel@gmail.com (N.Nedjah), laskri_n@yahoo.fr (N.Laskri),

Abstract- This research work aims at highlighting the importance of wastewater treatment generally and removing phosphorus from these waters specifically, in order to preserve our environment. Reducing the rejected quantity of phosphorus, nutrient element, in the receiving environments, enables the restriction of the phenomenon of water streams eutrophication. This is the primary objective of our research. Both the chemical and biological treatments are recognized as effective for phosphorus removal from waste water. In our study, we worked on phosphorus removal from urban wastewater through three treatments types: chemical, biological, and a combined one. The findings of the chemical treatment demonstrated a good treatment efficiency of the organic matter: 95% of DCO and 88% of phosphorus; as per the biological treatment: 60% of DCO and 49% of phosphorus were found. A further treatment has been conducted through combining the first couple of treatments. This combination method seeks to find the optimal dose of the different conventional coagulants namely lime, ferric chloride and aluminum sulfate .The combined treatment resulted in a better phosphorus removal efficiency: 83% of phosphorus and 96% of DCO. The obtained results proved to be highly encouraging and incite the responsible / heads of STEP to adapt and apply this type of treatment which revealed to be an appropriate purification technique of wastewater.

56

I/O Standards Based on Green Communication Using Fibonacci Generator Design on FPGA

Sumita Nagah[1], Bishwajeet Pandey[1], Kartik Kalia[1], Ravinder Kaur[1], Md. Saifur Rahman[2], Mahbub-ENoor[3]
[1]Gyancity Research Lab, New Delhi, India
[2]Noakhali Science and Technology University, Noakhali, Bangladesh.
[3]University of Barisal, Bangladesh
{sumi, gyancity}@gyancity.com, {kartikkalia4, rkrozy5, iamsaif07,mahbub0601001}@gmail.com

Abstract- In this paper LVCMOS, HSLVDCI, HSTL, LVDCI_DV2 and SSTL Input/output standard is used for the design of Green Fibonacci generator on 40nm FGPA to generate key for Wi-Fi Protected Access in order to make energy efficient communication. In naming convention of I/O standard, LV is low voltage, HS is high speed, DV2 is half impedance, CMOS is Complementary metal Oxide Semiconductor, DCI is digitally control impedance and SSTL is Stub series Transistor Logic. Here we used two frequencies ranging i.e. 1GHz and 10 GHz. After comparison it is observed that, LVDCI-DC2 is the most energy efficient and SSTL15 is the worst energy efficient on 1GHZ frequency where as SSTL15 and HSTL outperforms better on frequency range 10GHz. There is reduction in I/O power requirement of LVDCI is19.19% as compared to SSTL15 and SSTL15 shows 17.60 % reduction in energy on 10GHz as compared to LVDCI-DC2.

58

Hardware Implementation of an Eco-Friendly Electronic Voting Machine

GauravVerma, Amit Yadav, Sanjay Sahai, Utkarsh Srivastava, ShikharMaheswari, Karan Singh
Department of Electronics and Communication Engineering,
Jaypee Institute of Information & Technology, A-10, Sector 62, Noida (U.P.)-India.

Abstract- India is country of different cultures, economies, religion, social disparities and still India is world's largest democratic country. According to Indian democracy every person has the fundamental right to cast his/her vote to person of his/her choice. Before the use of voting machine people in India use to cast their vote (whether it is centre election or state election)by putting stamp in front of candidate's name and photo of their own choice, and then as per the prescribed format the ballot paper is folded and put into the Ballot box. This method takes lots of time in casting and even in counting of votes and also less secure and lots of errors are there. But introduction of Electronic Voting Machine (EVM) changed the whole procedure of casting a vote. EVM completely changed the voting procedure as there was no use of ballot boxes, ballot papers, and stamps, these all things converted to a Ballot unit of EVM. Thus EVM saved cost spend on transportation of large no of ballot boxes, cost spends on papers, cost spends on stamps etc. EVM is easy to store, maintain and transport. Errors of previous voting methods are removed like that of Invalid votes, time taken to casting votes reduced, thus very less problem compared to previous method of voting. Now counting is accurate with in much lesser time and no mischief on counting centre. This EVM is also eco-friendly in the sense it requires low voltage to operate and also replaces the tradition system which requires lots of paper work and manual operation.Keil u vision3 and Proteus software are used for this EVM.

60

Future Perspective and Current Aspects of Internet of Things Enable Design

Evedeep Kaur Bhatia[1] ,Simran Ohri[1],Gurbani Kaur[1] ,Minal Dhankar[1], Sweety Dabas[2]
Chitkara University, India, Gyancity Research Lab, India
{eva.bhatia93, simranohri10, gurbanikaur48, minal.dhankar, sweety.dabas}@gmail.com

Abstract- In this work, we are going to survey the latest progress in Internet of Things (IoTs) and also design IoTs enable electronics design like frame buffer, content addressable memory, and key generator for encryption and decryption. We are analyzing future perspective, overall impact, and its role in every corner of life, characteristics features and current aspects of IoTs. Apart from this, we study how this concept came into existence and its emergence changes our lives. In this paper, we have also designed IoTs enable Frame Buffer on FPGA for Object Tracking, IoTs enable Content Addressable Memory for processor and IoTs enable Key Generator for Green Communication. In order to make IOTs enable design, we are embedding a 128-bit Internet Protocol Version 6 address in each and every design.

61

Analysis of Thermal Stability of Energy Efficient Arithmetic Circuit Design on Different FPGA

Sehra Jindal, Prabhdeep Singh, Shreya Goel, Vivek Guraba,
Chitkara University
Punjab, India
{sehrajindal6, deepprabh95, shreyagoelsg}@gmail.com,
vguraba@hotmail.com,

Abstract- The paper involves discovering how the power dissipation of arithmetic circuits on FPGAs changes with the ambient temperature. We have covered 90nm, 65nm, 45nm, 40nm and 28nm technology based FPGA. The goal of the paper is to analyze the Power dissipation of arithmetic circuits on 23 FPGAs for 4 different temperatures. This has been done by checking the power dissipation of FPGAs by connecting them to XPower Analyzer which is a utility for estimating the power consumption and junction temperature of FPGA devices. The devices were connected to the XPower Analyzer which calculated power dissipation on different temperature as well as the total average power consumption and generated a report. Also the Percentage reduction in power when ambient temperature is scaled down is calculated. We are getting 20-90% reduction in power consumption, when we are using the most energy efficient FPGA available.

62

Energy Efficient Clean and Green IT: Concepts and Approaches

Kartik kalia[1], Deepa Singh Sisodiya[2] Dinesh Sharma[3], Vishok Singh[3]

Department of ECE, Chitkara University, Punjab[1]

ABV-IIITM, Gwalior[2]

IMS Unison University,

Dehradun[3]

kartikkalia4@gmail.com[1], deepasingh.iiitm@gmail.com[2]

vishok.singh@iuu.ac[3]dinesh.sharma@iuu.ac [3]

Abstract- Green IT practice is essential to minimize electricity bill. We have done our analysis on power consumption of computer. We have stated different management policies for reduction in energy consumption.Energy Star (ES) programme of the United States promotes energy efficiency in electronics products that provides an exceptional productivity as compared to the old or traditional systems. Energy Star program has been adopted by many countries to make a move towards Clean and Green environment. ES labels can be easily found on electronic appliances at homes, offices, buildings and many other places. Depending upon the devices, using these policies can result between 30%-90% of less power consumption. In our analysis, we got a reduction of 40% less power consumption in computers after implementing management policies. In this work, we are estimating power bill, and analyzing its economical feasibility along with that we are proposing a plan to reduce power consumption of academia and Institute. We have also discussed about management policies for disposal of e-waste.

69

Potential and Viability of Stand Alone Solar PV Systems for Rural Electrification of Pakistan by using RET Screen Software

Tauseef Akbar[1] Dr. AmjadUllah GussanMaaz Mufti[2]and Numan Khurshid[1]
University of Engineering and Technology,
Pakistan
National University of Sciences and
Technology, Pakistan
12gussanmufti@ces.nust.edu.pk

Abstract- Pakistan is facing energy crisis from last decade in spite having huge potential of solar energy. This research work will provide an assessment of the solar potential of Khyber Pakhtunkhwa (K.P.K) region. A comparison of the economic and financial analysis(Net Present Value, Internal Rate of Return, Payback period, and simple payback period) for a stand-alone PV systems for different regions of K.P.K have been done by simulating the solar systems on RET Screen. RET Screen has also been used for studying the effects of slope, latitude, orientation and geographical conditions of the selected six sites of K.P.K. Also, environmental effects such as Greenhouse gas (GHG) emission have been calculated and finally an optimum location for the installation of the solar panels has been proposed based on the results of the RET Screen.

71

Comparative Analysis between Multi-grid MEMS Structure and Inter-digital Electrodes for Moisture Measurement

Prakriti Kapoor [*1],Vishal Mehta [*2], Rahul Bansal [*3],
SatinderRana[#4],JatinderpalSingh #[5],Ajit Singh[#6]
*Chitkara University, Rajpura, [#]Surya World-Institute of Academic Excellence,Rajpura prakriti_kapoor@yahoo.co.in[1],
vishal.mehta@chitkara.edu.in[2]

Abstract- This paper describe design of novel sensor for moisture measurement that can be used in agriculture, automotive industries. In the present scenario moisture is measured by calculating change in relative permittivity which in turn depends upon change in capacitance of polymer layer sandwiched between electrodes. In this paper a new design is presented in which IDC sensor is used instead of Grid electrodes to calculate change in capacitance. Further, Comparative analysis has been done between these two topologies; device modeling has been carried out using COMSOL Multi-physics suite with MEMS approach.

74

Collaborative Optimal Reciprocal Collision Avoidance for Mobile Robots

Shehryar Ali Khan, Yasar Ayaz, Mohsin Jamil, Syed Omer Gillani, Muhammad Naveed, Ahmed Hussain Qureshi, Khawaja Fahad Iqbal.
RIME, SMME,
National University of Science & Technology (NUST), H-12, Islamabad, Pakistan.
shehryarali@smme.edu.pk

Abstract- Avoiding collision is one of the major research fields in mobile robotics. Various researchers around the globe are working on static and dynamic collision avoidance algorithms. One such algorithm is the Optimal Reciprocal Collision Avoidance that deals with multiple robots moving in a joint space without causing collision, that also without communicating and without centralized processing. This algorithm is very effective in handling collision avoidance. However, the problem of deadlock often appears when the robots have to navigate through densely crowded environments in joint space. The aim is to move robots in a small joint space and achieve collision avoidance without facing deadlocks. For this purpose we have extended this protocol into Collaborative Optimal Reciprocal Collision Avoidance to solve the problem of deadlocks. The protocol is inspired from the traffic rules and solves the problem of deadlocks effectively. The protocol was tested upon Player-Stage based simulation where deadlocks were avoided successfully.

75

Energy Efficient Memory Design Using Low Voltage Complementary Metal Oxide Semiconductor on 28nm FPGA

Sweety[1], Minal Dhankar[1], Ravinder S Kajal[1], Kartik Kalia[2], Kushagra Vashishta[2], Amit Kumar[3]
Department of Computer Science,
Maharaja Surajmal Institute, Janakpuri,
Delhi, India
Department of ECE, Chitkara
University, Punjab, India
Department of IT, IIIT Gwalior,
Gwalior, India
{sweety.dabas, minal.dhankar, kajalravi9, kartikkalia4, kushagravashishta, @gmail.com, advaita.amit }@gmail.com

Abstract — In this work, we are designing a energy efficient memory circuit on 28nm FPGA. Four different LVCMOS are used to validate the energy efficient design. There is 40.67% power reduction when LVCMOS25 is used in place of LVCMOS33. LVCMOS25 is better than LVCMOS33 IO Standard according to our experiment. With LVCMOS15 there is 75.70% total power reduction in compare with the LVCMOS33. LVCMOS15 is most energy efficient IO Standard and LVCMOS33 is most power consuming IO Standard. To design a power efficient memory we are using Verilog as HDL, Xilinx ISE 14.6 simulator with kintex-7 FPGA.

77

Power Consumption Analysis of BCD Adder Using XPower Analyzer on VIRTEX FPGA

G. Verma, Shambhavi Mishra, Sakshi Aggarwal, Surabhi Singh, Sushant Shekhar, Sukhbani Kaur Virdi
ECE Department, Jaypee Institute of Information Technology, NOIDA(U.P)-INDIA
gaurav.verma@jiit.ac.in, shambhavi2210@gmail.com.in, sakshi.agg05@gmail.com, surabhi.singh658@gmail.com, sushantshekhar09@gmail.com, sukhbanikaurvirdi3108@gmail.com

Abstract- Adders are the integral part of any digital circuit operation. Optimization of adder's supremacy along with its vicinity is a demanding chore. In this work an efficient BCD ADDER [1] is analyzed in terms of power consumption by scaling the various parameters like voltage, frequency and load capacitance. In addition to this the focus is also given on the airflow of the device to reduce the power. Finally the power is reduced by sending different encoded data at the input. The proposed designs are hardened and implement by means of VHDL and Xilinx ISE (integrated Software Environment) 14.5 and validated using XPower targeting Virtex FPGA. Power consumption is discussed in terms of clock, signals, logic, input/outputs and leakage. A comparative analysis has been shown at the end to validate the obtained results.

78

A Comparison of the 3DES and AES Encryption Standards

Noura Aleisa
n.aleisa@seu.edu.sa

Abstract- A comparison of two encryption standards, 3DES and AES is presented. It may seem that DES is insecure and no longer of any use, but that is not the case since the DES and 3DES algorithms are still beyond the capability of most attacks in the present day. However, the power of computers is increasing and stronger algorithms are required to face hacker attacks. AES has been designed in software and hardware and it works quickly and efficiently, even on small devices such as smart phones. With a large block size and a longer keys, AES will provide more security in the long term.

82

Thermally Aware LVCMOS Based Low Power Universal Asynchronous Receiver Transmitter Design on FPGA

Amanpreet Sandhu, Vidhoytma Gandhi, Simranpreet Kaur, Surbhi Huria, Divjot Singh, Wamika Goyal
Chitkara University, India[1]
Amanpreet.sandhu@chitkara.edu.in ,vidhoytma.gandhi@chitkara.edu.in
Simranchhabra2394@gmail.com, Surbhi.huria@chitkara.edu.in
divjotdivjot@gmail.com, wamika.goyal@gmail.com

Abstract- Green communication is the latest research trend practiced by researcher in green computing and network communication. There is no extensive work in green UART design. In order to fill this research gap, we are going to design LVCMOS based energy efficient Universal Asynchronous Receiver Transmitter (UART) that will create an avenue for IO standards based green communication. UART (Universal Asynchronous Receiver Transmitter) is a kind of serial communication protocol; mostly used for short-distance low speed, low-cost data exchange between computer and peripherals. Various energy efficient techniques have been applied to the design along with the change in IO standards. It has been concluded that there occurs 97.65% reduction in clock power, 75.14% reduction in I/O power, 7.19% reduction in leakage power, 17.37% reduction in junction temperature, and 71.12% reduction in total power dissipation in case SSTL2_II IO/standard, thus it is considered to be most energy and power efficient IO standard to be used in the future.

84

Analysis of Classical Controller by Variation of Inner-Loop and Controller Gain for Two-Level Grid-Connected Converter

Shahab Shahid Khawaja[1], Mohsin Jamil[1], Qasim Awais[2],Umer Asgher[1] and Yasar Ayaz[1]
Department of Robotics and Artificial Intelligence, School of Mechanical and Manufacturing Engineering, National University of Sciences and Technology,H-12 Main Campus, Islamabad, Pakistan.
University of Central Punjab, Lahore, Pakistan.
mohsin@smme.nust.edu.pk

Abstract- With the depletion of fossil fuel, the world is shifting towards the sources of alternate energy, but a major impediment in their utilization is their inter-connection with the grid. This paper builds on the model of a grid-connected converter which is used to interface the different alternate energy sources using Matlab/Simulink as simulation software. The classical control techniques proportional/proportional integral (P/PI) are applied on the model of the two-level grid-connected converter with LCL filter. The overall structure of the system is based upon the inner-loop capacitor current and outer-loop controller feedback. These parameters are varied and their effect is investigated in the presence of utility harmonics. The limitations and performance of the system with the variation in gain values is studied so that optimal gains can be identified.

85

WIRELESS POSITION TRACKING OF A DTMF BASED MOBILE ROBOT USING GSM AND GPS

Gaurav Verma, Himanshu Verma, Ipsita Singh, Aditya Vikram, Sheetal Singhal, Ashish Kumar,
Sandeep Banarwal, Khushhali Goel
Department of ECE, Jaypee Institute of Information Technology, Noida (U.P.)-India gaurav.verma@jiit.ac.in, himanshutechdn@gmail.com, ipsitasingh99@yahoo.in, adityavikram.6289@gmail.com, sheetalsinghal046@gmail.com, attach4ashish@gmail.com, banarwals@gmail.com, khushhali.k.goel@gmail.com

Abstract- The advent of new technologies has revolutionized the era of embedded system design in a way that every user is surrounded by smart devices (robots) which makes their life easier and comfortable. It has also been predicted by the researchers that by 2020, there will be billions of embedded devices talking to each other as compared to human beings termed as Internet of things (IOT). This paper is generally appropriated with the development of autonomous mobile robot used for wireless position tracking using GPS and sending that precise information on to a device such as mobile or tablet using GSM. This robot is equipped with GPS (for detection of location), GSM (for wireless data transfer), DTMF (for controlling robot with mobile or tab), sonar sensor (for obstacle detection) &flash light (for night vision). This mobile robot has wide variety of applications in industries like defense, aerospace, agriculture, & security etc. The basic functionality of the proposed design is simulated on proteus 7.1 and the complete design is implemented around ARM7 controller with required necessary interfaces.

86

THE EMERGING ELECTRONIC MEDIA AND ITS INFLUENCE ON THE READING HABIT OF SCHOOL CHILDREN IN NIGERIA

Agu Lilian Ebere
Institute of management and technology, IMT, Enugu, Nigeria
ebylilian4christ@yahoo.com

ABSTRACT : In our society today, the emerging electronic media is slowly taking a steady control over individual lives. The reading habit is fast vanishing into thin air (The Hindu, 2004). Students now lack the skill of reading. Reading of books or any other piece of written material in a quiet or peaceful corner of a library or home become an archaic idea for most school children and adults (The Hindu, 2004). Instead they spend more hours on electronic media. Browsing the net, online-chatting, playing with funky handsets and passing non-stop SMSs has become the order of the day. Shabi and Udofia (2009) noted that active learning from books is better than passive learning such as watching televisions and playing games.

87

SSTL Based Power Efficient Implementation of DES Security Algorithm on 28nm FPGA

Bishwajeet Pandey, Vandana Thind, Simran Kaur Sandhu, Tamanna Walia, Sumit Sharma
Chitkara University Punjab
gyancity@gyancity.com, vandanathind@gmail.com, simransandhu115@ymail.com,waliatamanna@gmail.com, sumitkaushal07@gmail.com

Abstract- In this particular work, we have done power dissipation analysis of DES algorithm, implemented on 28nm FPGA. We have used Xilinx ISE software development kit for all the observation done in this particular research work. Here, we have taken SSTL (Stub-Series Terminated Logic) as input-output standard. We have considered six sub-categories of SSTL (i.e. SSTL135, SSTL135_R, SSTL15, SSTL15_R, SSTL18_I and SSTL18_II) for four different WLAN frequencies (i.e. 2.4GHz, 3.6GHz, 4.9GHz, and 5.9GHz). We have done analysis considering five basic powers i.e. clock power, logic power, signal power, IOs power, leakage power and total power. There is 50-60% reduction in power dissipation, which is possible with proper selection of the most energy efficient IO standards i.e. SSTL135_R among SSTL logic families.

88

Wi-Fi to Li-Fi Migration accelerating for next generation systems: Approaches and applications

Hilal A. Fadhil
School of computer and communication Eng., University Malaysia Perlis (UniMAP), Malaysia

Abstract- The application of visible light communication (VLC) has grown in recent years for smart home technologies. Light-Fidelity (Li-Fi), an alternative to Wi-Fi that transmits data using the spectrum of pure visible light, Both Wi-Fi and Li-Fi transmit data over the spread spectrum, but whereas Wi-Fi used radio frequencies, Li-Fi uses visible light. This is a main advantage in that the visible light is far more plentiful than the radio spectrum and can achieve high efficiency. This paper proposed different approaches in order to implement the Li-Fi based VLC techniques. The proposed approaches are considered an efficient technology with superior bit-error rate (BER) performance in a typical smart home application.

90

Iterative Linear Quadratic Regulator (ILQR) Controller for Trolley Position Control of Quanser 3DOF Crane

Muhammad Faisal[1], Mohsin Jamil[1], Qasim Awais[2], Usman Rashid[1], Muhammad Sami, Syed Omer Gilani[1] , Yasar Ayaz[1] and Muhammad Nasir Khan[3]

Department of Robotics and Artificial Intelligence,
SMME, National University of Sciences and Technology,H-12 Main Campus, Islamabad, Pakistan.
University of central Punjab, Lahore, Pakistan, University of Lahore, Pakistan.
mohsin@smme.nust.edu.pk, qasim.awais@ucp.edu.pk

Abstract- In this paper, we have investigated the performance of iterative linear quadratic regulator (ILQR) on trolley position of 3 DOF crane. In ILQR, we select optimum parameters Q and R automatically instead of hit and trial method. Algorithm chooses the parameters Q and R which results in minimum trolley's settling time of the jib system. A number of simulations have carried out using Matlab/Simulink. The results show that the optimized LQR results reduce settling time of trolley along with smaller overshoot with less rise time.

91

Examination of Thai Construction Safety Factors using the Analytic Hierarchy Process

Thanwadee Chinda

School of Management Technology, Thammasat University, Muang Pathumthani 12000 Thailand

thanwadee@siit.tu.ac.th

Abstract- The construction industry is one of the industries with high accident rate. To improve safety standard to compete internationally, the key construction safety factors are examined in this paper utilizing the analytic hierarchy process. The results reveal the Policy factor as the most important factor to improve safety standard. The implementation plan must be practical and include regulations stated in the international safety standards.

92

Data Protection in Clouds using Two Stage Encryption

Pallav Sharma, Varsha Sharma, Sanjeev Sharma, Jitendra Agrawal
School of Information Technology, UTD, Rajiv Gandhi Proudyogiki Vishwavidhyalaya, Bhopal, India
pallav.20@gmail.com varshasharma@rgtu.net sanjeev@rgtu.net, jitendra@rgtu.net

Abstract- Cloud Computing has been an emergent technology that has opened the space for virtualization, as it provides many computational services and storage services over the Internet with the help of a browser. Cloud computing's core comprises of services like platform, infrastructure and software as a service. The unpredicted boom in cloud computing is driven by its simple economic benefit. It helps in reducing capital expense and minimizes operating expenses. This move however, has increased a major concern about the protection of data, as against the traditional system the data is now stored online and is far easily exposed than we realize. This raises a major security issue for data protection. Many techniques for protection of data have been proposed so far. However, the best available option till date is to encrypt user data before storing it over the cloud environment and decrypting it again before handing the data back to the cloud user. In this paper, we introduce a more efficient and stronger encryption process that allows a cloud service provider to protect user data more efficiently.

93

Optimization of Solar Photo Voltaic Power Generation Efficiency by Cooling System

Pankaj Jain, Sanjeev Sharma, Jitendra Agrawal
School of Information Technology, UTD, Rajiv Gandhi Proudyogiki Vishwavidhyalaya, Bhopal, India
pankaj@rgtu.net sanjeev@rgtu.net jitendra@rgtu.net

Abstract : Cooling of the Photovoltaic cells is a problem of great significance. The efficiency of waferbased crystalline as well as Solar cells gets reduced with increase of panel temperature. It is noted that the efficiency drops by about 0.4% for increase of 1° C of panel temperature. It is necessary to operate them at low temperatures in order to keep the PV module electrical efficiency at acceptable level. Therefore need for a low-cost cooling system for the Solar panels is felt. Water-cooling either by forced or natural flow, presents a non-expensive and simple method of PV cell cooling. This is already installed and operational at Energy Park of Rajiv Gandhi Proudyogiki Vishwavidyalaya (RGPV), Bhopal, India.

94

Developing an Efficient Desktop Application of Hospital Care Management System using Java and Database Management

Manisha Oswal, Mannat Nanda, Navreet Kaur
Department of Computer Science, Chitkara University, Chandigarh, India
Manisha.oswal56@gmail.com, mannatnanda@gmail.com,
rainavreet@gmail.com

Abstract- These days with the accelerated increase in human population, the amount of information and records is also becoming humongous in almost every aspect that may be considered. Handling such huge amounts of data has now become a backbreaking task. Handling involves – Inserting all the records accurately, displaying particular records according to the need, updating them as and when required and lastly deleting them when no longer of any use. These problems occur especially in large organizations where extensive amount of data is added and updated on a daily basis. We have considered one such organization that is Hospitals and have tackled this problem. We have worked on creating an efficient and user-friendly desktop application, which covers all aspects of data management with the help of Java on Net Beans IDE 7.3 as our front end and Microsoft SQL Server Management Studio asourbackend. This application makes data retrieval and handling incredibly easy to manage.

102

28nm FPGA Based Power Optimized UART Design Using HSTL I/O Standards

Isha Gupta, Garima, Swati Singh, Harpreet Kaur, Deepshikha Bhatt, Aamir Vohra
Chitkara University, India[1]
{isha.gupta, garima.turan, swati.singh, harpreet.kaur, deepshikha.bhatt }chitkara.edu.in, aamirvohra8@gmail.com

Abstract- UART abbreviated as Universal Asynchronous Receiver Transmitter is one of the essential element of communication system. It is being mostly used when there is a short-distance, between computer and peripherals. Whenever there is low-cost data exchange or the speed required for transmission is not high, UART's are also being used there. For the achievement of compact, stable and reliable data transmission, the implementation of UART with VHDL language can be integrated into FPGA. The Total power and Junction temperature of UART have been analyzed in the following paper when it is operating on different I/O standards of HSTL (HIGH SPEED TRANSCEIVER LOGIC) logic family and different range of frequencies from 1 GHz to 46 GHz. Analysis have also been done for two different 28nm FPGA's which helps to compare the total power reduction at two different FPGA technology so that the best suited FPGA for UART design consuming the least could be discovered. After analysis, it has been concluded that 91.96% of the total power can be saved in the case Kintex-7 and 91.98% of total power can be preserved in case of Artix-7 by operating the design at a frequency of 1 GHz.On the other hand the Junction temperature has been reduced to 11.84% in case of Kintex-7 and it has been reduced to 15.28% in case of Artix-7.

83

Two Level Voltage Source Grid Connected Inverter for Solar Photovoltaic **System**

Gussan Maaz Mufti [1]* Dr.Mohsin Jamil[1] Dr.Adeel Waqas[1]Muhammad Umer Ali[2]

[1]National University of Sciences and Technology (NUST) H-12 Islamabad, Pakistan

[2]University of Engineering and Technology, Pakistan

12gussanmufti@ces.nust.edu.pk

Abstract- In the recent years, the demand for the grid connected inverters has increased immensely as they act as an interface between the photo voltaic systems and the utility. The focus of this research article is to model and analyze the design characteristics of a two level, pulse width modulated, grid connected inverter using Matlab. The Proportional Integral and Proportional Resonant controller are being investigated and the performance of these controllers is being discussed. These simulation results show that the proportional resonant controller is able to mitigate the harmonics and perform satisfactory as compared to Proportional integral controller under the same harmonic conditions.

Our Next Conference:

Scopus Index RTCSE-2016, Malaysia

Welcome to the official website of International Conference on Recent Trends in Computer Science and Electronics Engineering (RTCSE'16). The conference will be held on 02-03 January 2016 in Kuala Lumpur, Malaysia. The main objective of RTCSE'16 is to present the research from different areas of science and technology. This conference provides a platform for researchers and scientists across the world to exchange and share their experiences and research results about all aspects of electronics and information technology. This conference also provides an opportunity to interact and establish professional relations for future collaboration. The conference aims to promote innovations and work of researchers, engineers, students and scientists from across the world on Advancement in electronic and computer systems. The basic idea of the conference is what more can be done using the existing technology. In Today's world electronic and computer systems plays an important role for future's innovation. These systems involve a very wide area for research.




We are pleased to invite prospective authors to submit their original manuscripts to RTCSE'16. **All accepted papers after registration will be published in following SCOPUS Index Journal:**

- International Journal of Software Engineering and Its Applications (IJSEIA)
- International Journal of Control and Automation (IJCA)
- Indian Journal of Science and Technology (IJST)
- International Journal of Applied Engineering Research (IJAER)
- International Journal of Multimedia and Ubiquitous Engineering (IJMUE)
- International Journal of Security and Its Applications (IJSIA)
- International Journal of Smart Home (IJSH)

International Conference on Recent Trends in Computer Science and Electronics Engineering (RTCSE), 02-03 January 2016 will be held in PARKROYAL Kuala Lumpur Jalan Sultan Ismail, 50250 Kuala Lumpur, Malaysia.

Kuala Lumpur is the national capital and most populous city in Malaysia. The city covers an area of 243 km2 (94 sq mi) and has an estimated population of 1.6 million as of 2010. It is among the fastest growing metropolitan regions in South-East Asia, in terms of population and economy.

Kuala Lumpur is a hub for cultural activities and events in Malaysia. Locals call Kuala Lumpur, the capital of Malaysia, KL. Its modern skyline is dominated by the 451m-tall Petronas Twin Towers, a pair of glass-and-steelclad skyscrapers with Islamic motifs. The towers also offer a public skybridge and observation deck. The city is also home to British colonial-era landmarks such as the Kuala Lumpur Railway Station and the Sultan Abdul Samad Building.

To know Malaysia is to love Malaysia - a bubbling, bustling melting pot of races and religions where Malays,
Indians, Chinese and many other ethnic groups live together in peace and harmony. Our multiculturalism has made Malaysia a gastronomical paradise and home to hundreds of colorful festivals. It's no wonder that we love celebrating and socializing. As a people, Malaysians are very relaxed, warm and friendly.

One of Malaysia's key attractions is its extreme contrasts, which further add to this theme of 'diversity'. Towering skyscrapers look down upon wooden houses built on stilts while five-star hotels sit just meters away from ancient reefs.

Rugged mountains reach dramatically for the sky while their rainforest-clad slopes sweep down to floodplains teeming with forest life. Cool highland hideaways roll down to warm, sandy beaches and rich, humid mangroves.

For the perfect holiday full of surprises, the time is now, the place is Malaysia.

At any time of the day, there's always something happening around Malaysia. Places to explore, food to feast on, shopping to indulge in, or festivals to celebrate – it's a non-stop adventure for everyone.

ISBN- 978-81-938900-0-4
Gyancity Research Lab Pvt Ltd
www.gyancity.com
gyancity@gyancity.com